REMARKS/ARGUMENTS

Claims 1, 3-14, 16-25 and 29-33 are currently pending in this application. Claims 1, 3-14, 16-25 and 29-33 are rejected. Claims 1, 12-22 and 23 have been amended and claim 11 has been canceled by the present response.

Rejections Under 35 U.S.C. §112

The Office Action rejected claims 11-14 and 16-21 under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, contending that "the specification fails to clearly link or associate the disclosed structure, material, or acts to the associating the physical queue with the ingress port in claim 11 line 11". (Office Action, page 2). Applicants respectfully disagree. However, to facilitate prosecution, the independent means plus function claim (claim 11) has been cancelled, and dependency has been amended for claim 11's dependent claims, so that they now depend from independent claim 22.

Rejections Under 35 U.S.C. §102(b)

The Office Action rejected claims 1, 3-14, 16-25, 29 and 31-33 (including each of the independent claims) under 35 U.S.C. §102(e) as being allegedly anticipated by U.S. Patent No. 7,046,687 to Brown et al. (hereinafter "Brown").

Applicants believe the claims in presently pending form are allowable. Nonetheless, to facilitate prosecution, Applicants have amended the independent claims to variably recite storing information associated with the packet "in the allocated physical queue, wherein the information comprises pointer information corresponding to a location of a payload of the packet, and wherein the payload for the packet is stored in a separate data structure from the physical queue".

The amendments to the independent claims are supported throughout the specification, including at pages 2-3 and 13-14, page 16, line 5 through page 17, line 10, and Fig. 2. Applicants reserve the right to assert the subject matter contained in the specification in this and other applications in the future.

Brown does not teach the above recited new claim feature.

As previously discussed, Brown does concern virtual queues, and it appears to describe the use of virtual queues in the context of facilitating transfer of data between the ports of a network device. "Configurable virtual output queues (VOQs) in a scalable switching system and methods of using the queues are provided. The system takes advantage of the fact that not all VOQs are active or need to exist at one time. Thus, the system advantageously uses configurable VOQs and may not dedicate memory space and logic to all possible VOQs at one time." (Brown, Abstract).

Brown uses the term "cell" to refer to a packet. It describes the use of virtual queues to store cells (i.e., packets) in the following manner: "The port processor 1100 in FIG. 11 A may have at least one VOQ in the set of VOQs 1110 *that stores cells* intended for each destination port 101 of the switch architecture 100 in FIG. 1 or the switch architecture 1000 in FIG. 10. If the switch architecture 100 in FIG. 1 or switch architecture 1000 in FIG. 10 has N number of destination ports 101, then each port processor 1100 may have at least N VOQs 1110 to receive incoming data cells." (Col. 23, lines 50-57 (emphasis added)). Brown continues: "FIG. 11B illustrates one embodiment of a plurality of VOQs 1130A 1130D within the set of VOQs 1110 in the port processor 1100 of FIG. 11A. Although only four VOQs 1130A 1130D are shown in FIG. 1B, the set of VOQs 1110 in the port processor 1100 of FIG. 11A may comprise any number of VOQs. In FIG. 11B, the *VOQ 1130A stores cells with a destination port address of 0* (e.g., destination port address bits=0000000000) *and a priority level of 0* (e.g., priority bits=000). The *VOQ 1130B stores cells with a destination port address of 0* (e.g., destination port address bits=0000000000) *and a priority level of 1* (e.g., priority bits=001). The *VOQ 1130C stores cells with a destination port address of 1* (e.g., destination port address bits=0000000001) *and a priority level of 0* (e.g., priority bits=000). The *VOQ 1130D stores cells with a destination port address of 1* (e.g., destination port address bits=0000000001) *and a priority level of 1* (e.g., priority bits=001). The destination port address and the priority level may comprise any configurable number of bits." (Col. 24, lines 1-19 (emphasis added)).

Based on the above sections of Brown, it is clear that Brown's virtual output queues store a "cell" (that is, a packet, including the payload of the packet) in each VOQ.

Brown's system does not provide for two separate data structures, a virtual output queue (embodied in a first data structure) where pointers corresponding to packets are stored, and another data structure, where the payloads of the packets are actually stored, the pointers corresponding to these locations, Rather, Brown describes a system with one data structure, in Brown's Fig. 11c, a RAM 1154, for example, which appears to hold the "cells", i.e., the packets at issue. Brown does indicate the presence in some embodiments, for example, in embodiments where "each VOQ 1130 . . .is a circular queue" (Brown, col. 24, lines 44-45, and Fig. 11B), of head pointers and tail points for the each VOQ, and Brown also describes a Free List head pointer and tail pointer. However, regarding the locations of those pointers, Brown merely suggests that they might be located in registers. It makes no mention of the physical locations of those registers, but from its Figures, it appears that the registers are located on the same data structure (the RAM) as the plurality of VOQs.

By contrast, in various embodiments of the claimed invention, the physical queues which correspond to each VOQ are located in one data structure, and the payload of the packet is stored in another location. The independent claims, as amended, recite "storing information associated with the packet in the allocated physical queue, wherein the information comprises pointer information corresponding to a location of a payload of the packet, and wherein the payload for the packet is stored in a separate data structure from the physical queue". As stated in the specification, "Packets are stored in random access buffers associated with the ingress ports. However, only pointers to the data need to be stored in the respective VOQs; the payloads may be stored elsewhere (e.g., in an off-chip random access memory). (Specif., page 2, line 34, to page 3, line 4). The specification further states: "In preferred implementations, 'assigning' the first packet to the first queue involves storing classification information and pointer information for the first packet in the first free queue. (Specif., page 13, line 32, to page 14, line 3).

For at least the above reasons, Applicants respectfully submit that independent claims 1, 22 and 23 are patentable over Brown, and request that the Examiner withdraw his section 102(e) rejections against these claims, as well as the claims that depend upon them.

Claim Rejections under 35 U.S.C. §103(a)

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown in view of Ciancaglini et al. (U.S. Publication No. 2005/0089054), hereinafter "Ciancaglini". Claim 30 depends on independent claim 1.

For the reasons discussed above, Brown does not teach or suggest the features of the independent claims. Applicants have reviewed Ciancaglini and it does not cure the deficiencies of Brown. Accordingly, for at least the reasons stated above, Applicants respectfully submit that claim 30 is also patentable over the cited references.

Conclusion

In view of the foregoing reasons, it is respectfully submitted that all claims are allowable. Should the examiner believe that a telephone conference would expedite the prosecution of this application, applicant's attorney requests that the examiner contact him at the telephone number below.

Applicants hereby petition for any (additional) extension of time that may be required to maintain the pendency of this case, and any required fee for such extension or any further fee required in connection with the filing of this amendment is to be charged to Deposit Account No. 504480 (Order No. ANDIP035US/425565).

Respectfully submitted,
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